SHAYAUN BASHAR

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EDUCATION

University of California, San Diego Sep 2019 – June 2024

Bachelor of Science, Electrical Engineering, Provost Honors 22'

Relevant Courses: Digital IC Design, Active Circuit Design, Advanced Digital Design Project, Software foundation I & II, Programming for Data Analysis

SKILLS

Software Tools: Altium Designer, Cadence Virtuoso/Spectre, Quartus Prime, Ansys HFSS, LTSpice

Programing Languages: C++, SystemVerilog, Python, freeRTOS, Cuda

Technical: VNA testing, EE lab tools (Oscilloscope, Function Gen., Multimeter), Communication Protocols(UART, I2C), Soldering, 3D printing

PUBLICATION/AWARDS

- "**ForceSticker: Wireless, Batteryless, Thin & Flexible Force Sensors**"(Co-Author) ACM IMWUT '23
- "Design and Evaluation of a miniaturized Force Sensor Based on Wave Backscattering" (Co-Author) IEEE RA-L, IROS '22
- "PaciForce" (Co-Presenter) (Won Best Poster Award in ECE Dept. at UC San Diego's Research Expo 2025)

WORK EXPERIENCE

Qualcomm Institute Aug 2024 – Present

R&D Engineer I, Advisors: Dinesh Bharadia and James Friend, WCSNG Lab

- Designed an embedded force/vacuum sensor into a pacifier to replace the subjective "gloved finger" test, providing clinicians with quantitative data for diagnosing newborn feeding issues.
- Built and tested multiple prototypes using **PCBs** and **3D-printed** fixtures; developed **Python** scripts to control **VNA**/**Arduino**/force actuator, automate S11 data collection while step forces applied, and generate calibration curves for sensitivity/linearity analysis.
- Optimized sensor fabrication by developing a custom hysteresis-free silicon mixture and refining geometry/polymer design, increasing yield by 80%, reducing fabrication time by 25%, improving frequency consistency by 80%, and enhancing robustness from 300 to 10,000 cycles.

PROJECTS

ForceSticker: Wireless, Battery-less, Thin & Flexible Force Sensors April 2021 – March 2023

Undergraduate Researcher/Intern, WCSNG Lab UC San Diego, Advisors: Dinesh Bharadia and Tania Morimoto

- Developed a 900 MHz wireless, battery-less force sensor with a novel capacitive design that converts applied force into analog phase shifts in backscattered RF signals for low-power industrial and medical use.
- Led technical efforts in designing flex PCB in **Altium/HFSS**, simulating performance in **HFSS**, performing sensor fabrication, PCB soldering, and **VNA** testing for antenna and circuit verification
- Commercialization efforts by completing NSF I-Corps regionals and IGE MedTech Accelerator Programs

SHA256/Bitcoin Hashing Algorithm RTL Model in System Verilog September 2023 – December 2023

ECE 111 (System Verilog Design course) Final Project

- Designed and implemented a pipelined SHA-256 hashing engine in SystemVerilog on Quartus Prime, verifying correctness through simulation and testbench development.
- Applied the design to Bitcoin's double-hash algorithm using parallelized nonce-based computation, optimizing FSM sequencing and balancing parallelism vs. clock frequency to improve throughput under hardware constraints.

Custom 8-bit Adder (45 nm CMOS using Cadence Virtuoso**)** April 2023 – June 2023

ECE 165 (VLSI course) Final Project

- Designed a high-speed 8-bit parallel-prefix adder (Kogge-Stone architecture); implemented transistor-level dynamic logic and verified functionality/timing through **Cadence Spectre** simulations.
- Architected the carry-tree using PG, FCO, and PPC blocks; performed tradeoff analysis between speed, area, and power across static vs. dynamic CMOS implementations, achieving multi-GHz operation with low fan-out delay.
- Completed schematic, layout, and simulation flow (**DRC/LVS + Spectre transient analysis**), presenting results in ISSCC-style report format.

Self-Made SQL Database (C++) March 2024 – June 2024

ECE 141B Course Project

- Designed and implemented a multi-layer C++ architecture (App → Query Processing → Block Storage) using object-oriented principles and design patterns for modularity, extensibility, and clean separation of concerns.
- Developed a block-based persistence layer with Table-of-Contents indexing and LRU caching, optimizing storage efficiency and performance while adhering to SOLID design principles.